REMARKS

The Office Action dated August 15, 2005 has been carefully considered. Claims 1-18 are pending. Reconsideration and allowance are respectfully requested in light of the following remarks. Claim 17 has been amended in this Response.

Applicants respectfully submit that the present Office Action contains a defect under 35 C.F.R. § 1.104(b). The present Office Action is not "complete as to all matters" because Claim 18 has not been examined by the Examiner. *Id.*. Applicants submitted a Preliminary Amendment (Exhibit B) with an R.C.E. (Exhibit C), as shown by the received postcard from the U.S.P.T.O. (Exhibit A). This Preliminary Amendment (Exhibit B) contained a new Claim 18, which was not examined in the present Office Action. Applicants have called this error to the attention of the Office within one month of the mail date (August 15, 2005) of this Office Action. Therefore, Applicants respectfully request that the Office restart the previously set period for reply to run from the date the error is corrected as required under M.P.E.P. 710.06.

Claim 17 stands objected to because of an informality. Accordingly, the language "execution pipeline" has been replaced by the language "execution *unit*." Applicants contend that the rationale underlying this amendment bears no more than a tangential relation to any equivalence in question because the language has been added merely to correct a typographical error. *Festo Corp. v. Shoketsu Kinzoku Kogyo Kabushiki Co.*, 122 S.Ct. 1831 (2002).

Applicant does not believe that any fees are due; however, in the event that any fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of Carr LLP.

Should the Examiner deem that any further amendment is desirable to place this Application in condition for allowance, the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

Dated: 9/14/05

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Gregory W. Carr
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The "Received" stamp of the Patent and Trademark Office imprinted hereon acknowledges the filing of:

☑ RCE Transmittal Form ☑ Fee Transmittal Form ☑ CHECK $ 990.00 ☑ AMENDMENT (13 pages) ☐ Extension of Time Request: ___ Months ☐ Information Disclosure Statement ☐ Response to Missing Parts/Incomplete Appl'n	☐ Assignment Papers ☐ Drawings ☐ Petition ☐ Power of Attorney ☐ Status Letter ☐ OTHER: _____
NAME OF INVENTOR(S)/APPLICANT: Christopher Michael Abernathy, et al.	SERIAL NO.: 10/042,082
TITLE: Method and Apparatus for Dynamic Power Management in an Execution Unit Using Pipeline Wave Flow Control	(PTO USE ONLY)
DOCKET NO.: AUS920010807US1 (IBM 2335000)	
Date Mailed: 6/24/05 ☑ Cert/Mailing ☐ Express Mail: (attach sticker) ATTY/PRLG/SECY: GWC/ DMM /bde	

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Abernathy et al. §

Serial Number: 10/042,082 §

Filed: January 7, 2002 §

Group Art Unit: 2116

For: METHOD AND APPARATUS FOR DYNAMIC POWER MANAGEMENT IN AN EXECUTION UNIT USING PIPELINE WAVE FLOW CONTROL §

Examiner: Tse W. Chen

Mail Stop RCE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450

CERTIFICATE OF MAILING

I hereby certify that the original paper identified herein is being deposited with United States Postal Service as first class mail, postage prepaid, to Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450

on: 6/24/05

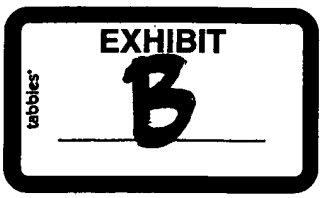
Bradley D. Ellis

Bradley D. Ellis

AMENDMENT

Dear Sir:

In connection with a Request for Continued Examination filed herewith, Applicants respectfully request the Examiner to enter the Amendment filed May 20, 2005, and then to consider the following Amendment:



CLAIMS

1. (Previously Presented) A microprocessor configured for executing at least one instruction, the microprocessor having a main processor clock, the microprocessor comprising:

a first stage having one or more storage components configured for storing operand data of the at least one instruction, the first stage being clocked by at least a first clock derived from the main processor clock;

a first combinatorial logic connected to the first stage for receiving the operand data from the first stage and configured for processing the operand data and generating first output data, wherein the first clock is operational only during a first period of time when the operand data is processed by the first combinatorial logic;

a second stage of one or more storage components configured for storing the first output data, the second stage being clocked by at least a second clock derived from the main processor clock;

control logic that is at least configured to:

generate at least one instruction-valid control bit, wherein the at least one instruction-valid control bit is configured to selectively disable only the first clock derived from the main processor clock if a first stage is unused or to disable only the second clock derived from the main processor clock if a second stage is unused; and

a second combinatorial logic connected to the second stage for receiving the first output data from the second stage and configured for processing the first output data and generating second output data, wherein the second clock is operational only during a second period of time when the first output data is processed by the second combinatorial logic.

2. (Original) The microprocessor of Claim 1, further comprising:

a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time;

a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time.

3. (Original) The microprocessor of Claim 1, further comprising:

a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time;

a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time; and

a dynamic clock-control unit connected to at least the first local clock buffer for providing a first control signal to at least the first local clock buffer and configured for generating the first control signal, the first control signal enabling the first clock signal to be operational only during the first period of time.

4. (Original) The microprocessor of Claim 1, further comprising an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic.

5. (Original) The microprocessor of Claim 1, further comprising:

an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic;

a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time; and

a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time.

6. (Original) The microprocessor of Claim 1, wherein the first stage comprises one or more latches, and wherein the second stage comprises one or more latches.

7. (Original) The microprocessor of Claim 1, further comprising an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic, wherein the integrated storage component comprises an array.

8. (Original) The microprocessor of Claim 1, wherein the second period of time is automatically determined by delaying the first period of time by one cycle of the main processor clock.

9. (Original) The microprocessor of Claim 1, further comprising:

an integrated storage component configured for storing the operand data, the integrated storage component being connected to the first stage for providing the operand data to the first stage and being connected to the second combinatorial logic for receiving the second output data from the second combinatorial logic;

a first local clock buffer connected to the first stage for providing at least the first clock to the first stage only during the first period of time;

a second local clock buffer configured for generating the second clock and connected to the second stage for providing at least the second clock to the second stage only during the second period of time; and

a dynamic clock-control unit connected to at least the first local clock buffer for providing a first control signal to at least the first local clock buffer and configured for generating the first control signal, the first control signal enabling the first clock signal to be operational only during the first period of time.

10. (Original) The microprocessor of Claim 1, wherein each storage component in the first stage comprises:

a master latch configured for storing the operand data and being clocked by a first master clock derived from the first clock; and

a slave latch connected to the master latch for receiving the operand data from the master latch and storing the operand data, the slave latch being configured for being clocked by a first slave clock derived from the first clock.

11. (Previously Presented) A method for dynamically reducing power consumption in a microprocessor configured for executing at least an instruction, the microprocessor having a main processor clock, the method comprising the steps of:

storing operand data in a first stage of one or more storage components residing in the microprocessor, the first stage being clocked by at least a first clock derived from the main processor clock;

transmitting the operand data from the first stage to a first combinatorial logic residing in the microprocessor, wherein the first clock is operational only during a first period of time when the operand data is processed by the first combinatorial logic;

processing the operand data in the first combinatorial logic;

generating first output data from the first combinatorial logic;

storing the first output data in a second stage of one or more storage components residing in the microprocessor, the second stage being clocked by at least a second clock derived from the main processor clock;

transmitting the first output data from the second stage to a second combinatorial logic residing in the microprocessor, wherein the second clock is operational only during a second period of time when the first output data is processed by the second combinatorial logic;

processing the first output data in the second combinatorial logic;

generating second output data from the second combinatorial logic;

generating an instruction-valid control bit;

in response to the instruction-valid control bit, reducing power consumption in the microprocessor by dynamically controlling the first and second clocks by selectively disabling at least one local clock buffer to prevent switching of only the first clock or only the second clock.

12. (Original) The method of Claim 11, further comprising the steps of:

transmitting at least the first clock from a first local clock buffer to the first stage only during the first period of time;

generating the second clock from a second local clock buffer; and

transmitting at least the second clock from the second local clock buffer to the second stage only during the second period of time.

13. (Original) The method of Claim 11, further comprising the steps of:

transmitting at least the first clock from a first local clock buffer to the first stage only during the first period of time;

generating the second clock by a second local clock buffer;

transmitting at least the second clock from the second local clock buffer to the second stage only during the second period of time.

generating a first control signal;

transmitting the first control signal from the dynamic clock-control unit to at least the first local clock buffer; and

enabling the first clock signal by the first control signal to be operational only during the first period of time.

14. (Original) The method of Claim 11, further comprising the steps of:

storing the operand data in an integrated storage component residing in the microprocessor;

transmitting the operand data from the integrated storage component to the first stage; and

transmitting the second output data from the second combinatorial logic to the integrated storage component.

15. (Original) The method of Claim 11, further comprising the steps of:

transmitting at least the first clock from a first local clock buffer to the first stage only during the first period of time;

generating the second clock from a second local clock buffer;

transmitting at least the second clock from the second local clock buffer to the second stage only during the second period of time;

storing the operand data in an integrated storage component residing in the microprocessor;

transmitting the operand data from the integrated storage component to the first stage; and

transmitting the second output data from the second combinatorial logic to the integrated storage component.

16. (Original) The method of Claim 11, further comprising the steps of:

transmitting at least the first clock from a first local clock buffer to the first stage only during the first period of time;

generating the second clock from a second local clock buffer;

transmitting at least the second clock from the second local clock buffer to the second stage only during the second period of time.

generating a first control signal by a dynamic clock-control unit residing in the microprocessor;

transmitting the first control signal from the dynamic clock-control unit to at least the first local clock buffer;

using the first control signal to enable the first clock signal to be operational only during the first period of time;

storing the operand data in an integrated storage component residing in the microprocessor;

transmitting the operand data from the integrated storage component to the first stage; and

transmitting the second output data from the second combinatorial logic to the integrated storage component.

17. (Previously Presented) A method for dynamic power management in an execution unit using pipeline wave flow control having multiple stages with clocks interconnected thereto comprising:

storing operand data in a first stage of one or more storage components residing in the execution pipeline;

transmitting the operand data from the first stage to a first combinatorial logic residing in the execution unit, wherein the clock of the first stage is operational only during a first period of time when the operand data is processed by the first combinatorial logic;

processing the operand data in the first combinatorial logic;

generating first output data from the first combinatorial logic;

storing the first output data in a second stage of one or more storage components residing in the execution pipeline;

transmitting the first output data from the second stage to a second combinatorial logic residing in the execution unit, wherein the clock of the second stage is operational only during a second period of time when the first output data is processed by the second combinatorial logic;

processing the first output data in the second combinatorial logic;

generating second output data from the second combinatorial logic;

generating an instruction-valid control bit;

in response to the instruction-valid control bit, reducing power consumption in the execution unit by dynamically controlling the first and second clocks by selectively disabling at least one local clock buffer to prevent switching of only the first clock or only the second clock.

18. (New) A microprocessor configured for executing at least one instruction, the microprocessor having a main processor clock, the microprocessor comprising:

a first stage having one or more storage components configured for storing operand data of the at least one instruction, the first stage being clocked by at least a first clock derived from the main processor clock;

a first combinatorial logic connected to the first stage for receiving the operand data from the first stage and configured for processing the operand data and generating first output data, wherein the first clock is operational only during a first period of time when the operand data is processed by the first combinatorial logic;

a second stage of one or more storage components configured for storing the first output data, the second stage being clocked by at least a second clock derived from the main processor clock;

control logic that is at least configured to:

generate at least two instruction-valid control bits, wherein the at least two instruction-valid control bits are configured to:

disable the first clock derived from the main processor clock by a first instruction-valid control bit if a first stage is unused or to disable the second clock derived from the main processor clock by a second instruction-valid control bit if a second stage is unused;

enable the first clock and the second clock in response to a scan mode signal;

disable the first clock by the first instruction-valid control bit in response to a first stop control signal and disable the second clock by the second instruction-valid control bit in response to a second stop control signal; and

a second combinatorial logic connected to the second stage for receiving the first output data from the second stage and configured for processing the first output data and generating second output data, wherein the second clock is operational only during a second period of time when the first output data is processed by the second combinatorial logic.

REMARKS

Applicants have filed on May 20, 2005, an Amendment in response to the Office Action dated March 31, 2005. In consideration of the Advisory Action dated June 6, 2005, Applicants herewith submit a Request for Continued Examination (RCE) and a further amendment presenting new Claim 18.

Applicants have now made an earnest attempt to place this Application in condition for allowance. For the foregoing reasons and for other reasons clearly apparent, Applicants respectfully request full allowance of Claims 1-18.

Applicants enclose a check in the amount of $990.00 for payment of the fee under 37 C.F.R. 1.17(e) for a Request for Continued Examination, and for payment of the fee under 37 C.F.R. 1.17(h) for one independent claim in excess of three. Applicants do not believe that any other fees are due; however, in the event that any other fees are due, the Commissioner is hereby authorized to charge any required fees due (other than issue fees), and to credit any overpayment made, in connection with the filing of this paper to Deposit Account No. 50-0605 of CARR LLP.

****

Should the Examiner deem that any further amendment is desirable to place this application in condition for allowance. the Examiner is invited to telephone the undersigned at the number listed below.

Respectfully submitted,

CARR LLP

Dated: 6/24/05

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PTO/SB/30 (04-05)
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Request for Continued Examination (RCE) Transmittal

Address to:
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Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Application Number	10/042,082
Filing Date	01/07/2002
First Named Inventor	Abernathy
Art Unit	2116
Examiner Name	Tse W. CHEN
Attorney Docket Number	AUS920010807US1 (IBM 2335000)

This is a Request for Continued Examination (RCE) under 37 CFR 1.114 of the above-identified application.
Request for Continued Examination (RCE) practice under 37 CFR 1.114 does not apply to any utility or plant application filed prior to June 8, 1995, or to any design application. See Instruction Sheet for RCEs (not to be submitted to the USPTO) on page 2.

1. Submission required under 37 CFR 1.114 Note: If the RCE is proper, any previously filed unentered amendments and amendments enclosed with the RCE will be entered in the order in which they were filed unless applicant instructs otherwise. If applicant does not wish to have any previously filed unentered amendment(s) entered, applicant must request non-entry of such amendment(s).

   a. [✓] Previously submitted. If a final Office action is outstanding, any amendments filed after the final Office action may be considered as a submission even if this box is not checked.

      i. [ ] Consider the arguments in the Appeal Brief or Reply Brief previously filed on _____

      ii. [✓] Other Amendment filed May 20, 2005.

   b. [✓] Enclosed

      i. [✓] Amendment/Reply

      ii. [ ] Affidavit(s)/ Declaration(s)

      iii. [ ] Information Disclosure Statement (IDS)

      iv. [ ] Other _____

2. Miscellaneous

   a. [ ] Suspension of action on the above-identified application is requested under 37 CFR 1.103(c) for a period of _____ months. (Period of suspension shall not exceed 3 months; Fee under 37 CFR 1.17(i) required)

   b. [ ] Other _____

3. Fees The RCE fee under 37 CFR 1.17(e) is required by 37 CFR 1.114 when the RCE is filed.

   a. [✓] The Director is hereby authorized to charge the following fees, any underpayment of fees, or credit any overpayments, to Deposit Account No. 50-0605. I have enclosed a duplicate copy of this sheet.

      i. [✓] RCE fee required under 37 CFR 1.17(e)

      ii. [ ] Extension of time fee (37 CFR 1.136 and 1.17)

      iii. [✓] Other Extra claim fee (37 CFR 1.16(h))

   b. [✓] Check in the amount of $ 990.00 enclosed

   c. [ ] Payment by credit card (Form PTO-2038 enclosed)

WARNING: Information on this form may become public. Credit card information should not be included on this form. Provide credit card information and authorization on PTO-2038.

EXHIBIT C

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT REQUIRED

Signature	Gregory W. Carr	Date	6/24/05
Name (Print/Type)	Gregory W. Carr	Registration No.	31,093

CERTIFICATE OF MAILING OR TRANSMISSION

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Mail Stop RCE, Commissioner for Patents, P. O. Box 1450, Alexandria, VA 22313-1450 or facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

Signature	Bradley D. Ellis		
Name (Print/Type)	Bradley D. Ellis	Date	6/24/05

This collection of information is required by 37 CFR 1.114. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Mail Stop RCE, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.